



Research Center

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SLVS Test Chip for the MIPI Physical Layer

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Abstract:

The MIPI (Mobile Industry Processor Interfaces) Alliance standardizes a number of interfaces inside a mobile device. The MIPI D-PHY is a scalable, low-power, high-speed physical layer upon which several MIPI standards, like camera and display interfaces, are based. The serial data transmission is using the SLVS signaling method

A test chip designed by Nokia Research Center Bochum proves now the potential of this signaling method for high-speed and low-power data transmission. Whereas the bi-directional link runs up to 1.2 Gbps on an unshielded flex PCB, it still consumes less than 10mW in total, which is an excellent value. Four wires per direction transfer differential Strobe and Data signals.

The chip has been designed as full custom design, using Texas Instruments' latest 65nm process technology. The major building blocks are a serializer / deserializer, comma detection, physical media access as well as additional control and test logic. The active chip area is 0.01mm². First samples have been extensively tested and show full functionality.

Index Terms:

MIPI

physical layer

SLVS

high speed serial data transmission

serializer

deserializer

INTRODUCTION

High speed serial data links are going to replace more and more parallel interfaces today. There are certain drawbacks with the classical parallel CMOS interfaces:

- A great number of lines (wires) is needed
- High pin count becomes a limiting factor for ICs
- High power consumption of single-ended CMOS interfaces
- Skew between clock line and data lines limits the maximum speed

High speed serial connections can solve some of the above mentioned problems. For device to device connections, serial links are already very common (e.g. USB, Ethernet). But also inside devices, like a mobile phone, the need for a serial connection between different integrated circuits on a printed circuit board is evolving. IC pin count constraints, board space limitations due to miniaturization as well as flexible lines going over the hinge in a clamshell phone are the main drivers.

Expanding this item it can be found, that even serial connections of several dies inside a multichip package and sometimes even inside a single integrated circuit make sense [1]. Work has already been done in that area, which led to widely accepted standards like e.g. PCI express. Anyhow those solutions are not optimized for mobile devices because of their relatively high power consumption and implementation complexity.

The MIPI (Mobile Industry Processor Interfaces) Alliance was founded by ARM, Nokia, ST Microelectronics and Texas Instruments and contains more than 90 companies today. It standardizes a number of interfaces inside a mobile device which were proprietary before, with a focus on low power consumption at high transmission speed. A number of them are based on the same physical layer (D-PHY), just with specific protocol layers on top.

A key feature of the MIPI D-PHY is the signaling method, called SLVS (Scalable Low Voltage Signaling). This paper presents shortly the basics of SLVS in section II. The building of the SLVS test chip is described in section III. Measurement results of the chip follow in section IV. Finally, a conclusion and outlook is given in section V.

The SLVS System

The potential of the MIPI D-PHY to achieve high bit rates with a low power consumption is based to a large extent on its signaling method, which is known as scalable low voltage signaling (SLVS). Fig.1 shows a schematic of an SLVS-200 connection.

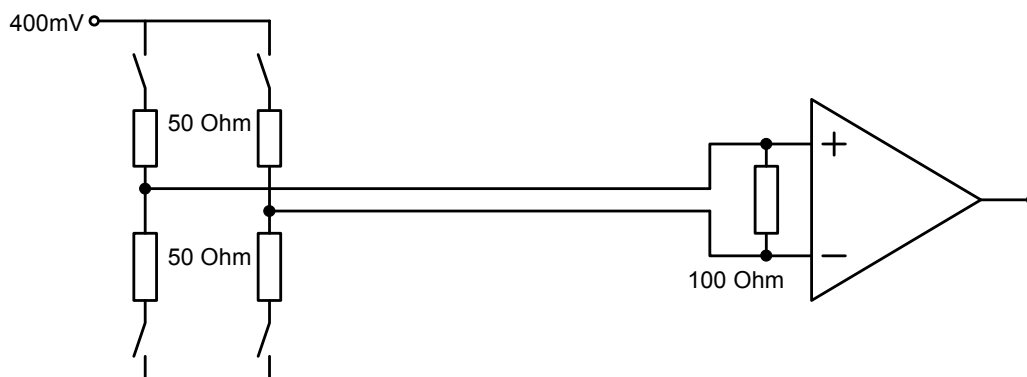


Fig. 1: The SLVS is a differential signaling method

SLVS uses differential signaling with resistive line termination on both ends. Differential signaling is known to be more robust and less sensitive against noise than single-ended signaling [2]. The twofold termination eliminates reflection at both the driving and receiving end of the link, leading to improved signal integrity. The voltage swing on a single line is 200mV which results in a 400mV differential swing. This is a good compromise between power consumption and noise immunity for the given

environment in a mobile terminal. It is also low enough to cope with the voltage limitations in new integrated circuit technologies for the next 10 years.

SLVS-200 is based on the JESD8-13 SLVS-400 standard that has been published by JEDEC in October 2001 [3].

The signal current is taken from a 400mV voltage source. It flows through a source resistor of 50 Ohm into the line. At the receiver the current is terminated into a 100 Ohm resistor and fed to the return line. The return line is terminated by another 50 Ohm resistor to ground. Thus the nominal signal current is 2mA DC.

The Test Chip

The target of the test chip was to prove the usability of the SLVS signaling for high-speed data transfer in a mobile phone. In order to get meaningful and future-proof results, a state-of-the-art silicon technology with a feature size of 65nm was selected. The test chip has a total die size of one square millimeter but is heavily pad limited due to a great number of pads for test purposes. The active area is about 0.01mm². It is assembled in a 64 pin VFQFPN package.

The chip contains the RX and TX path in order to allow demonstrating a full bidirectional link. Each path has a low speed parallel interface to the higher protocol layers and the high speed serial interface. The serial interface uses two differential pairs per direction: One pair for the “Strobe” and one for the “Data” signal.

The functionality of the chip can be divided into three parts, which will be described in the next sections.

The Transmitter

Fig. 1 shows a block diagram of the transmitter path.

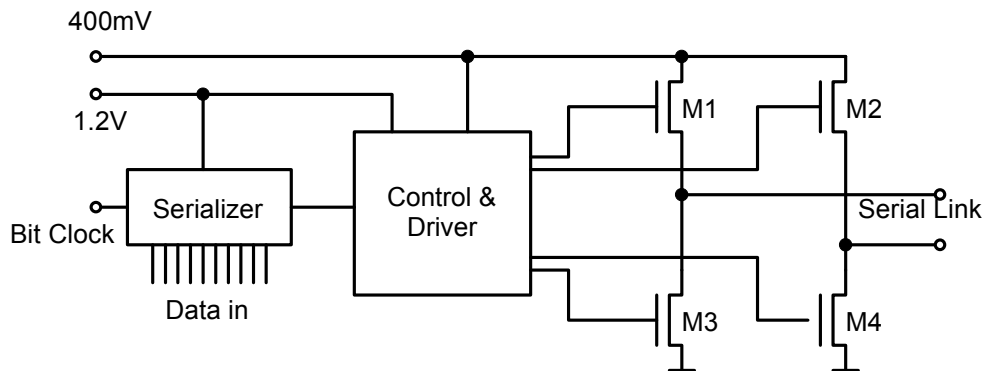


Fig. 1 The transmitter path. Only one TX PMA cell (M1..M4) is shown for simplicity

The data enter the chip with 10 bits in parallel. They are serialized using a ten-bit serializer. The high-speed bit clock for the serializer is supplied by an external clock generator to allow flexible testing with different bitrates. When implemented in the final application IC, the bitclock will be provided by an internal PLL circuit. The serial data go through control logic and pre-drivers to a physical media access cell (PMA). This generates the differential signals for the SLVS lines.

An H-bridge of four NMOS transistors is used inside the PMA. Only NMOS transistors are used even for the high side switch. In this way a better matching between the driver strength of the low side and the high side is achieved. This allows impedance matching of the H-bridge transistors without passive resistors. Passive resistors are not available in some digital processes and often suffer from large tolerances. Therefore they are avoided as far as possible in this design.

The H-Bridge is controlled by a driver circuit. It consists of a logic that creates the four control signals for the H-bridge, as well as a booster that drives the large gate capacitance of the H-bridge transistors.

There are multiplexers inserted between many stages in the signal chain to allow to either sense or force the signal for test purposes. By doing so, each block can be tested separately in case of faulty behavior, enabling effective debugging.

The Receiver

The receiver chain is shown in Fig. 2.

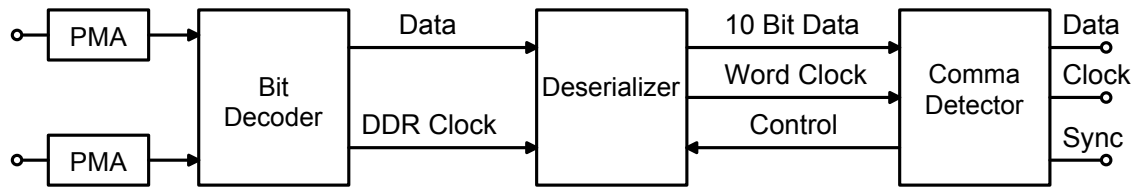


Fig. 2 The receiver path.

The differential signal enters the chip at the receiver PMAs, one carrying the Data and the other one the Strobe signal. The serial data stream goes to a deserializer that creates a parallel data stream. The bitclock for the deserializer (double data rate clock) is extracted from the link by XORing the Data and Strobe signals. It is then further divided by a frequency divider to a word clock which is used as a qualifier for the outgoing parallel data. A comma detector is attached to the deserializer to synchronize on the symbol boundaries with the aid of special comma symbols. To make this possible, the transmitted data need to be encoded. In the present test application, this is performed with the well-known 8b10b coding scheme.

The data leave the chip on ten parallel lines and are available there for further processing by the higher protocol layers (data link layer etc.). As done in the transmitter, also the receiver contains multiplexers between each block in order to ease testing.

The RX physical media access cell contains a termination resistor, a differential amplifier and an output signal driver. The termination resistor is divided into two resistors with a capacitive coupling to ground in the center (Fig. 3). By doing so, the receiver achieves better noise immunity and common mode rejection ratio.

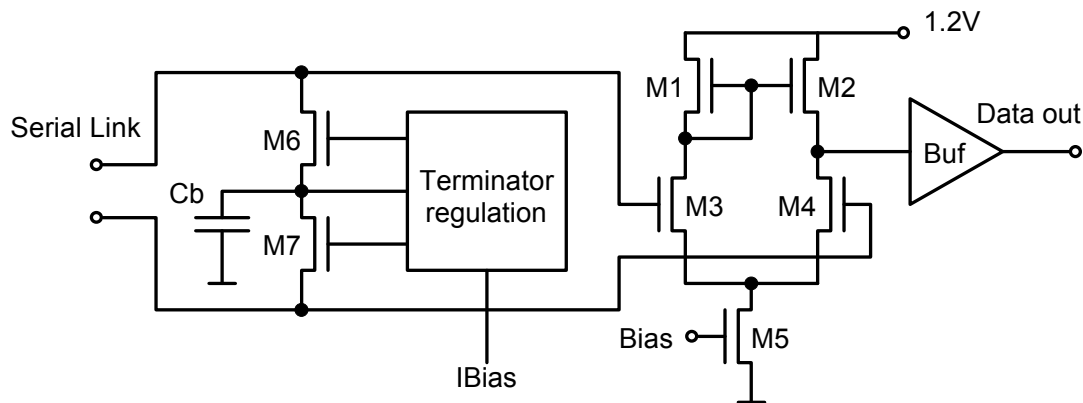


Fig. 3 Receiver PMA with Terminator

The NMOS transistors M6 and M7 are used for the termination instead of passive resistors for the already mentioned reasons. The center voltage on the decoupling capacitor C_b in Fig. 3 is fed to a control network that creates the required gate voltage for the termination transistors. By doing so, they can always be kept in linear range even when the common mode signal on the link varies due to temperature or manufacturing tolerances.

Test and control circuits

In addition to the already mentioned multiplexers, the chip contains a pseudo random bit pattern generator. This can be used for testing purposes and allows easy monitoring of eye diagrams on the lines without requiring any external data generators.

All multiplexers as well as various other control signals are controlled by a 48 bit shift register that can be accessed via a serial programming interface (SPI) from outside the chip. This enables a variety of different tests.

Design methodology

The chip was built as a full-custom mixed-signal ASIC. Due to the tight timeframe it was very important to perform efficient simulations: Accurate enough to find any mistakes but also as fast as possible to not delay the project.

The analog cells, like drivers, amplifiers and biasing networks were simulated accurately with TI

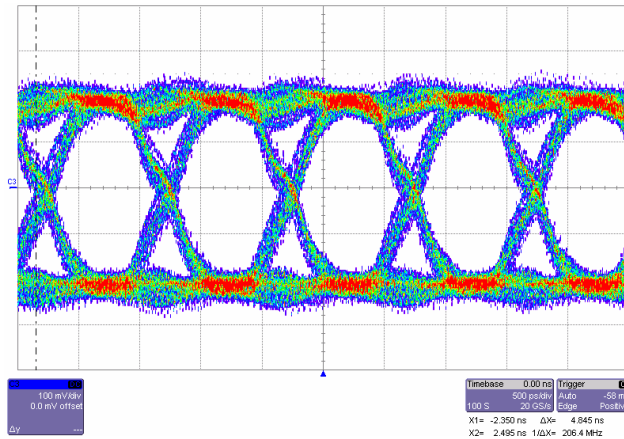


Fig. 6 Eye diagram measured with 20cm flexible PCB

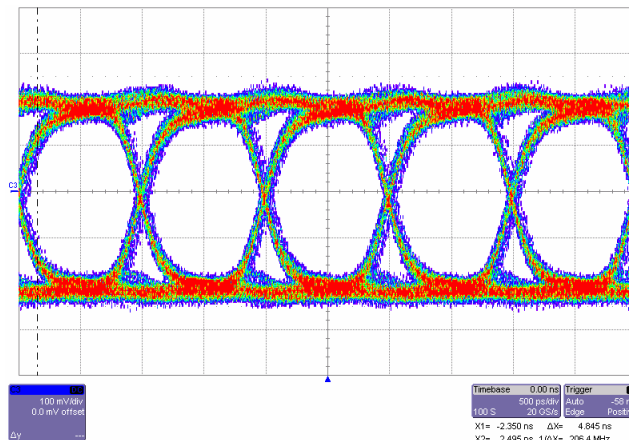


Fig. 7 Eye diagram measured with 100cm CAT5 cable

It can be observed that the multilayer PCB with 50 Ohm tracks shows the best performance, which has been expected. The flex PCB shows the worst performance since it is a very cheap single layer unshielded type. Anyhow even this shows a reasonable performance.

TABLE 1 MAXIMUM LINK SPEEDS IN SLVS MODE

Medium	PCB	Flex	Cable
Speed MBit/s	1400	1200	1300

Table 1 shows the maximum data rate for the different link media.

The power consumption of the link is divided in two parts. The power of the analog part of the link is nearly speed independent because of the constant current flow in an SLVS system. It is taken from a 400mV supply.

The power consumption of the digital logic is speed dependant. It is taken from a 1.2V supply. The test chip allows measuring the two currents separately. Table 2 shows the currents of the analog and digital parts at different speeds.

TABLE 2: POWER CONSUMPTION OF THE LINK

Speed MBit/s	100	300	500	700	900
Analog (mA)	3,9	4,0	3,95	3,92	3,97
Digital (mA)	0,29	0,52	0,76	0,99	1,22
Sum (mW)	1,91	2,22	2,49	2,76	3,05
pJ/Bit	19,10	7,40	4,98	3,94	3,39

The given values are for a unidirectional link (one transmitter and one receiver). A complete bidirectional link consumes double the power and transfers double the amount of bits per second.

Conclusion

This paper described the development and measurement of a test chip to proof the abilities of the SLVS signaling method. The chip has been measured under various conditions, showing that the functionality of the chip is correct and the performance meets (respectively exceeds) the targeted values.

It is possible to achieve more than 1 Gbps speeds with a Data / Strobe encoded serial transmission and SLVS signaling, using a straight-forward (not yet optimized) design. Note that the MIPI D-PHY uses SLVS signaling, but a different clocking method.

To exploit the full advantage of SLVS voltage definitions, voltage-mode drivers were used in the design. This enables the lowest possible power consumption, compared to the often used current-mode drivers. This is an important point to notice, since many silicon and IP vendors might be tempted to re-use the traditional current-mode driver circuits from e.g. LVDS also for the MIPI D-PHY. This approach would result in interface implementations which are functionally in order but would not reach the best energy efficiency.

In this 65nm CMOS process, the dynamic power consumption of the main digital blocks like serializer and deserializer can be held at very moderate levels, even at 1 Gbps speed. The presented design was straight-forward, using standard gates, put together with a handcrafted layout. With older silicon processes, some optimization is surely needed to achieve very high speeds. Eventually the use of special logic gates (like current mode logic, CML) is beneficial.

It was observed in the measurements that mismatch of line impedance is not extremely critical, even at high speeds. This is an advantage of the SLVS system, which has near-end and far-end termination, in contrast to other systems which have only far-end termination.

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